IMPRINTED INTEGRATED CIRCUIT SUBSTRATE AND METHOD FOR IMPRINTING AN INTEGRATED CIRCUIT SUBSTRATE

Ronald Patrick Huemoeller
Sukitano Rusli

FIELD OF THE INVENTION

The present invention relates generally to semiconductor packaging, and more specifically, to An imprinting method and an imprinted substrate for providing electrical and mechanical connection to integrated circuit dies.

BACKGROUND OF THE INVENTION

Semiconductors and other electronic and opto-electronic assemblies are fabricated in groups on a wafer. Known as "dies", the individual devices are cut from the wafer and are then bonded to a carrier. The dies must be mechanically mounted and electrically connected to a circuit. For this purpose, many types of packaging have been developed, including "flip-chip", ball grid array and leaded grid array among other mounting configurations. These configurations typically use a planar printed circuit etched on the substrate with bonding pads and the connections to the die are made by either wire bonding or direct solder connection to the die.

The resolution of the printed circuit is often the limiting factor controlling interconnect density. Photo-etch and other processes for developing a printed circuit on a substrate have resolution limitations and associated cost limitations that set the level of interconnect density at a level that is less than desirable for interfacing to present integrated circuit dies that may have hundreds of external connections.

As the density of circuit traces interfacing an integrated circuit die are increased, the inter-conductor spacing must typically be decreased. However, reducing inter-conductor spacing has a disadvantage that migration and shorting may occur more frequently for lowered inter-conductor spacings, thus setting another practical limit on the interconnect density.

Therefore, it would be desirable to provide a method and substrate having improved interconnect density with a low associated manufacturing cost. It would further be desirable to provide a method and substrate having reduced susceptibility to shorting and migration between conductors.

SUMMARY OF THE INVENTION

An imprinted substrate and a method for imprinting a substrate use imprinting to generate a circuit pattern within a substrate. A substrate is embossed using a tool formed in the

shape of the desired circuit pattern and conductor is applied to the embossed pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a pictorial diagram depicting a substrate and a tool for embossing in accordance with an embodiment of the invention;

Figures 2A-2D are pictorial diagrams depicting various stages of preparation of a substrate in accordance with an embodiment of the invention;

Figure 3 is a pictorial diagram depicting an integrated circuit in accordance with an embodiment of the invention;

Figures 4A-4F are pictorial diagrams depicting various stages of preparation of a substrate in accordance with an alternative embodiment of the invention;

Figure 5 is a pictorial diagram depicting an integrated circuit in accordance with an alternative embodiment of the invention;

Figures 6A-6C are pictorial diagrams depicting various stages of preparation of a substrate in accordance with alternative embodiments of the invention; and

Figures 7A-7C are pictorial diagrams depicting various stages of preparation of a substrate in accordance with other alternative embodiments of the invention.

The invention, as well as a preferred mode of use and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein like reference numerals indicate like parts throughout.

DETAILED DESCRIPTION

Referring now to the figures and in particular to Figure 1, a substrate 13 and an embossing tool 10 in accordance with an embodiment of the present invention are depicted. Embossing tool 10 is used to form substrate 13 in a novel process that permits embedding circuits beneath the top surface of substrate 13 and isolating the circuits in channels. Embossing tool 10 comprises a machine having a plate 11 for supporting a thin metal tool foil 12. Tool foil 12 is stamped to form an outline that conforms to a reverse image of desired contour of the top of substrate 13 after processing. A force F is applied between substrate 13 and plate 11 and the substrate material flows to conform to the contour of tool foil 12. Substrate 13 comprises a resin layer 14 that is deformable by the above-described embossing technique and a backing layer of copper 15. While the embodiment of Figures 1 depicts single-sided embossing of a substrate having a backing layer, other embodiments of the invention extend to stand-alone substrates embossed from a resin

material having no backing layer. Both single-sided and double-sided embossing processes may be used and the resulting circuits may form plated-through holes, embedded circuit traces, etched circuit traces and vias. All of the techniques illustrated in the embodiments of the invention may be applied to both sides of a substrate that has no backing layer, or has resin layers deposited on both sides of a metallic backing layer. Suitable materials for an embossable substrate are plastic resins such as PLASKON SMT-B-1RC, NITTO HC100XJAA or Liquid Crystal Polymers (LCPs) such as Rogers R/MAX 3700, R/MAX 3800, BIAC CC, or SUPEREX.

The embossing tool foil can be made with existing processes that are used in the formation of stamps for manufacturing compact discs (CDs). In the CD manufacturing process, metal foil is stamped using a master that is created for the production of multiple foils. The foils are then attached (embedded) in a polymer resin to support the foils. To support the process of the present invention, metal foils can be made in the same manner, but may be reused.

Referring now to figure 2A, the first stage in the preparation of substrate 13 in accordance with an embodiment of the present invention. Substrate 13A has been deformed by tool foil 12 such that voids and indentations in accordance with the figure are generated in resin layer 14. Referring now to figure

2B, copper plating 16 is seed plated or electrolytically deposited on the surface of substrate 13A to form plated substrate 13B. Next, as depicted in Figure 2C, a permanent etchant resist material is applied to substrate 13B and is planed to conform to the top of copper plating 16. Then, as illustrated in Figure 2D, the copper plating 16 is etched and the permanent resist is removed, leaving a circuit channel 16A and a conductive post mounting area 16B for mounting a flip chip mechanical bonding post. Circuit channel 16A can be used for electrically connecting terminals of a flip-chip package, or may be circuit traces extending out of the plane of the figures for routing circuit traces.

While the figures illustrate two conductive circuit channels 16A, the figures are depicting only a portion of the total substrate. More than a hundred circuit channels 16A will generally be used in an integrated circuit design and may be oriented in any direction within the surface of substrate 13. Additionally, materials other than copper may be used, depending on the process used. For example if etching is not necessary for a particular circuit, gold foil may be applied to the channels formed in an embossed substrate. The present invention provides a process for forming circuits within channels in a substrate that are below the top surface of the substrate. This an improvement over the present state of the art, which generally

provides only surface conductors. The channels formed by embossing place the conductors below the surface and the conductors are thereby insulated from adjacent conductors by the substrate.

Referring now to Figure 3, an integrated circuit 30 in accordance with an embodiment of the invention is depicted. A flip-chip die 31 having electrical terminal posts 32 and a mounting post 34 is attached to substrate 13D by a solder ball 35. The solder ball provides electrical and thermal connection from flip-chip die 31 to substrate 13D via post mounting area 16B formed from remaining copper conductor 16. Channels 16A contact electrical terminal posts 32, providing contact to the electrical terminals. Since the circuits forming channels 16A may extend in the plane of the figure to any point on substrate 13D, routing of the electrical connections to terminal posts 32 may be made to other locations on substrate 13D. Multiple dies may be mounted on substrate 13D and the channels 16A used to interconnect the various dies.

Referring now to Figure 4A, an alternative embodiment of the present invention is depicted. Following the process of Figures 2A-2C, substrate 13C may be prepared in an alternative process to that illustrated above. Substrate 13C of Figure 2C is coated on both sides with a photo-sensitive etch resist material 41. Next as illustrated in Figure 4B, portions of etch resist

material 17 is removed by an imaging process, exposing copper plating 16 in areas for subsequent plating. Then, as illustrated by Figure 4C, the exposed areas of copper plating 16 are plated with a material resistant to chemical etchant such as nickel/gold to form wire bonding pads 42. The remaining photo-etch resist material 17 is removed, yielding substrate 13G of Figure 4D. Circuit material 16 is then etched to remove the portions uncovered by permanent etch resist, forming channels 16B and interconnect 16C of substrate 13H of Figure 4E. Finally, the permanent etch resist material is removed, leaving the prepared substrate 13J of Figure 4F.

Referring now to Figure 5, an integrated circuit 50 is depicted in accordance with an alternative embodiment of the invention. Prepared substrate 13J is connected to a die (not shown) by wires 51 that are bonded to wire bonding pads 42, providing an electrical connection to the die. A ball grid array (BGA) solder ball is applied to the plated area 42A on the backside of substrate 13J and is electrically connected to wire bonding pads 42 via interconnect 16C. Solder ball 35A provides an electrical terminal for external connection to other circuits as in a typical BGA arrangement. Channels 16B are used to route connections within substrate 13J and may provide connection to flip-chip mounted dies in accordance with the earlier-described

embodiment of the invention, forming a substrate that embodies both embodiments of the present invention.

Referring now to Figure 6A, an alternative double-sided substrate preparation is disclosed in accordance with an embodiment of the invention. Embossing tool 10B comprises a machine having a top plate 11A for supporting a thin metal tool foil 12A for forming the top of substrate 13K. Tool foil 12A is stamped to form an outline that conforms to a reverse image of desired contour of the top of substrate 13K after processing. Embossing tool 10C comprises a machine having a bottom plate 11B for supporting a thin metal tool foil 12B for forming the bottom of substrate 13K. Tool foil 12B is stamped to form an outline that conforms to a reverse image of desired contour of the top of substrate 13K after processing. A force F is applied between embossing tool 10B and embossing tool 10C, embossing substrate 13K so that the substrate material flows to conform to the contour of tool foils 12A and 12B. Substrate 13K as depicted comprises a top resin layer 14B and a bottom resin layer 14C deposited over a metal layer 15A of copper. The metal layer is perforated by an resist-etch process or other means, so that plated through holes may be made through substrate 13K, but a double-sided substrate may be embossed without metal layer 15A or with multiple metal layers. Metal layer 15A may be used to

provide an electrical and thermal conductive path for devices mounted on substrate 13K after the substrate is prepared.

Referring now to Figure 6B, substrate 13L is depicted after embossing in accordance with Figure 6A. Depressions are made through substrate 13L for generation of plated-through holes, through to metal layer 15A for contact vias to metal layer 15A, and within resin layer 14B for circuit traces. Substrate 13L is then plated by depositing metal, adding etch resist and then etching as described above for single-sided substrates. Referring now to Figure 6C, the final plated substrate is depicted. Plated-through hole 17B provides insulation from the metal layer 15A, since the embossing process removed an area of substrate 13L that was smaller in diameter than the perforation in metal layer 15A, but contact could be made with metal layer 15A for other plated-through connections. Via 17C provides contact to metal layer 15A from one side of substrate 13L and traces 17C provide circuit paths. Many combinations of embossing and etching may be used to provide multi-layer substrates with or without incorporated metal planes.

Referring now to Figure 7A, an alternative double-sided substrate preparation without a metal layer is disclosed in accordance with yet another embodiment of the invention. Embossing tool 10D comprises a machine having a top plate 11C for supporting a thin metal tool foil 12C for forming the top of

substrate 13M. Tool foil 12C is stamped to form an outline that conforms to a reverse image of desired contour of the top of substrate 13M after processing. Embossing tool 10E comprises a machine having a bottom plate 11D for supporting a thin metal tool foil 12D for forming the bottom of substrate 13M. Tool foil 12D is stamped to form an outline that conforms to a reverse image of desired contour of the top of substrate 13M after processing. A force F is applied between embossing tool 10D and embossing tool 10E, embossing substrate 13M so that the substrate material flows to conform to the contour of tool foils 12C and 12D. Substrate 13M as depicted comprises only a resin layer without metal layers.

Referring now to Figure 7B, substrate 13N is depicted after embossing in accordance with Figure 7A. Depressions are made completely through substrate 13N for generation of plated-through holes, and within substrate 13N for circuit traces. Substrate 13N is then plated by depositing metal, adding etch resist and then etching as described above for single-sided substrates.

Referring now to Figure 7C, the final plated substrate is depicted. Plated-through hole 17D and circuit traces 17E and 17F have been added via the plating and selective etching processes described above for the single-sided embodiment of the invention.

The above description of embodiments of the invention is intended to be illustrative and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the above disclosure and fall within the scope of the present invention.